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Full transceiver circuit simulation using VHDL-AMS

This paper describes the successful simulation of a complete transceiver circuit with the new VHDL-AMS standard. The aim was to verify the functionality and connectivity of a complete RF transceiver chip under actual application conditions. The transceiver circuit is dedicated to E-GSM/GPRS standards for mobile phone applications. At such a level of complexity, traditional tools do not allow simulation of the design at transistor level. In addition to digital models, mixed-signal behavioural models of the transmitter, receiver and frequency synthesiser have been developed for a high level of abstraction, as required in a top-down methodology. The complete simulation of the chip took 23 minutes of CPU time for 6ms of circuit operation. For the first time we were able to verify and debug such a circuit at the top-level.

Full chip verification seems to be the most critical concern for analogue mixed-signal (AMS) designers today. How can they perform the final check when all functions are put together and are limited by simulation speed performance? From the digital top-down design approach, where behavioural modelling with HDL languages such as VHDL and Verilog play an essential role in dealing with high complexity, comes a similar methodology that can be applied to AMS design.

The new mixed-signal HDL standard VHDL1076.1 (called VHDL-AMS) gained approval in March 1999 [1], being a superset of the existing VHDL standard with AMS extensions. Designers can now build complex analogue and mixed-signal models by combining differential equations, algebraic constraints and logical controls. Conventional digital VHDL constructs can be used in concert with the new analogue and mixed-signal extensions.

ADVance MS (ADMS) from Mentor Graphics [2] is the first single kernel mixed-signal simulation environment to support VHDL-AMS together with all existing HDL standards VHDL, Verilog, Verilog-A and also SPICE. By merging behavioural with SPICE level modelling, ADMS provides designers with an unprecedented flexibility and a new design approach. It enables intelligent trade-offs by choosing detailed models for high accuracy and behavioural models for simulation speed performance. Today, not only can designers perform full chip verification at the top-level, they can also perform design architecture experimentation, tolerate late-stage design changes and facilitate design re-use.

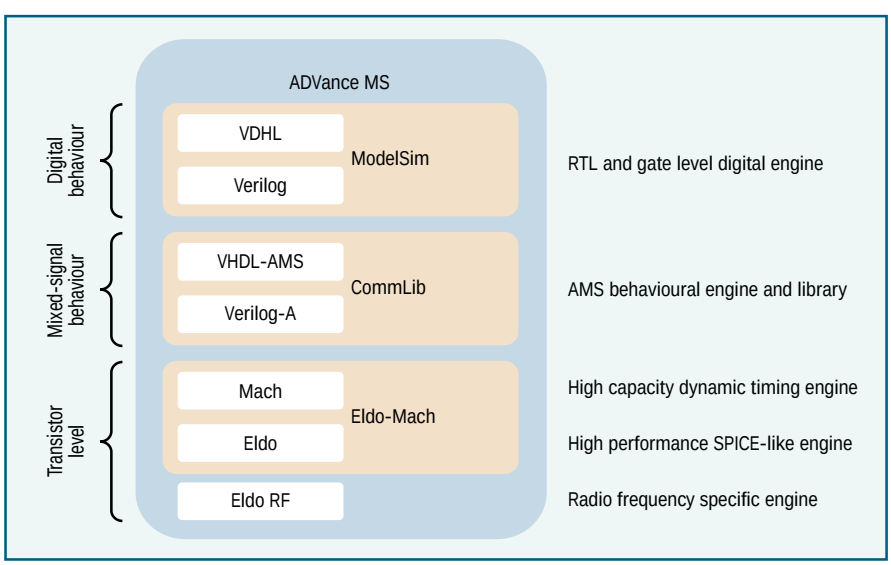

Figure 1: ADVance MS mixed signal simulator

AFRICA Circuit Description

STMicroelectronics (STM) has developed a complex E-GSM/GPRS standards transceiver chip named AFRICA. Since the performance of traditional tools diminishes and do not allow the complete system verification at transistor level, designers were attempting to overcome excessive simulation run times by using a VHDL-AMS behavioural modelling approach. The simulator selected was ADMS from Mentor Graphics.

The transceiver is composed of four major blocks:

- Receiver including low-noise amplifiers (LNA), down-conversion mixers and low-pass filters (LPF)
- Transmitter including low-pass filters, up-conversion mixers and power amplifiers (PA)
- Frequency synthesizer including charge pump (CP), phase detector (PFD), voltage-controlled oscillator (VCO) and fractional-N phase-locked loop (PLL) functions
- Programmable digital control block

The circuit is a zero intermediate fre-

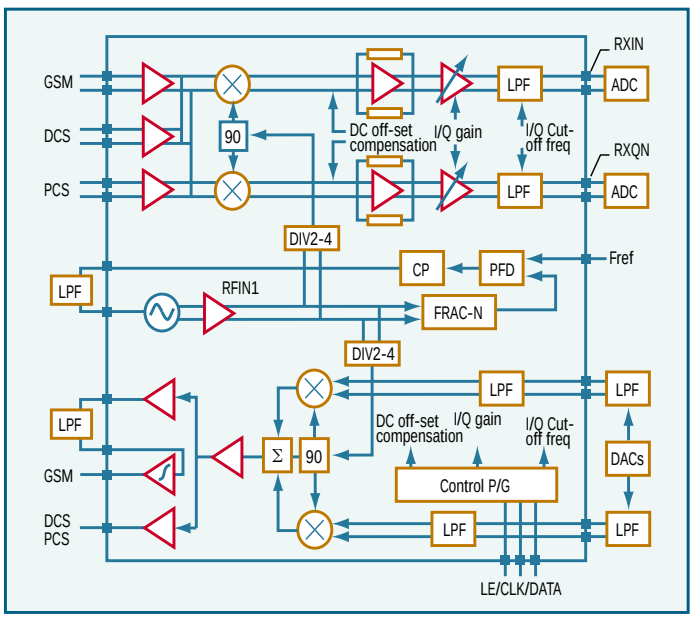

Figure 2: AFRICA block diagram

quency (ZIF) half-duplex transceiver [3]. In reception mode, the radio frequency (RF) waveform is directly down-converted into a baseband (BB) signal by mixer circuits. The baseband signal is amplified by a gain stage and transformed by a low-pass filter before becoming the output signal of the chip that feeds the external analogue-to-digital converters (ADC).

In transmission mode, the baseband signal from an external digital-to-analogue converter (DAC) is up-converted into an RF signal by mixer circuits. The power stage provides some gain to the RF signal before delivering it to the external power amplifier.

The up-conversion and down-conversion principle used in the circuit is based on the following timing (t) equation:

$$A_1 * SIN(2\pi f_{RF} * t+\phi_1) * A_2 * SIN(2\pi f_{LO} * t+\phi_2)$$

for a receiver.

Where A_1, f_{RF} and ϕ_1 represent amplitude, frequency and phase of the RF signal, and A_2, f_{LO} and f_2 likewise represent the local oscillator (LO) signal.

The baseband frequency can then be extracted follows:

$$f_{BB} = f_{LO} - f_{RF}$$

In this GSM circuit, the baseband frequency is ranging from 1KHz to 100KHz and the local oscillator (LO) is as high as 4GHz. The large frequency ratio between BB and LO of at least four thousand times is a real challenge for transient simulation. In order to look at one period of the BB signal, the designer has to run up to 40,000 clock cycles of the LO. Needless to say, this has a major impact on simulation run time.

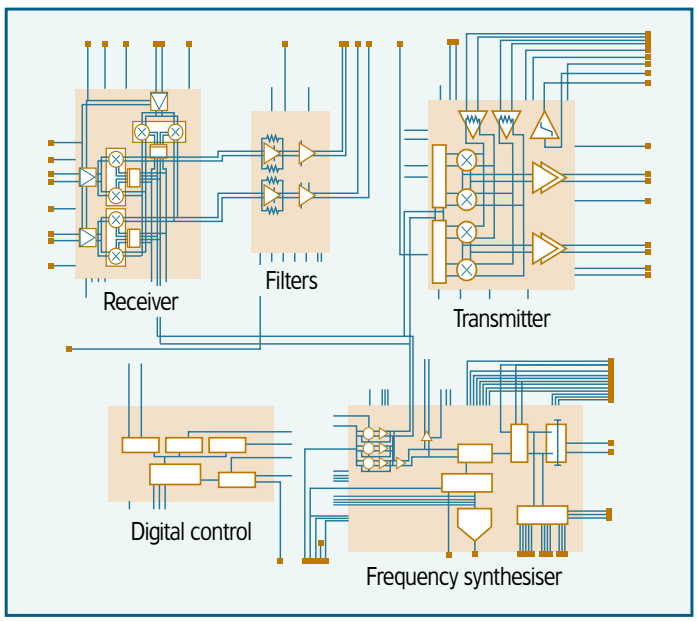

Figure 3: AFRICA circuit partitioning

Our objectives

Under time-to-market pressure, we look for new approaches in order to reach our ultimate goal: first silicon success. Essentially we try to reduce the number of design cycles by detecting and eliminating as many flaws as possible during the design phase. The objectives for the AFRICA project are as follows:

- Full chip functional verification
- Full chip connectivity verification
- Test mode simulation

As each block of the system has already been designed, qualified and optimised separately by traditional tools, our new approach is to deal with the top-level of the system. There is no need for detailed information and accuracy at the transistor level. But we want to ensure that the chip responds correctly to the programming sequence.

Connectivity verification errors are frequent in spite of its relative simplicity. Bus connection inversion can cause a very expensive chip failure. The ports of each model should be checked against the connectivity of the corresponding schematic block. A standard SPICE netlist has been used in this case.

The third objective is to improve our test process. We want to use the simulation to evaluate the testability, prepare the test vectors and extract signals to be used in the test phase.

Our new approach is to adopt behavioural modelling using VHDL-AMS for time domain simulation. We have selected the ADMS simulator because of its language neutral strategy. The simulator not only supports VHDL-AMS, but all HDL standards down to SPICE and C. It is also important for us to be able to assemble different intellectual property (IP) blocks of different standards.

Modelling strategies

From the schematic representation of the circuit, we first need to partition the design into the following functional sub-blocks:

- Receiver
- Transmitter
- Baseband filter
- Frequency synthesiser
- Digital control

Then we develop, at the highest possible level, behavioural models of these sub-blocks using VHDL-AMS. Only the digital block is represented by a Verilog gate level netlist. This partitioning corresponds to the first hierarchical level of the circuit.

The major modelling difficulty is to handle the high frequency of the RF signal in a time domain simulation. It is clear that dealing with such a signal at 4GHz leads directly to a non-acceptable simulation run time.

If we examine closely the RF signal path in the circuit, we notice that the signal remains at the radio frequency only at very limited times. More over, this RF signal is always sampled at the LO frequency and quickly converted into baseband for all other cases. Our idea is to look for an equivalent RF mathematical representation that allows us to rebuild the internal BB signal. This approach should allow us

Figure 4: Digital block simulation results

to deal only with the baseband and hence to avoid the frequency ratio problem.

Following is the mathematical representation of an ideal sinusoidal waveform:

$$A_{(t)} * SIN(2\pi f_{(t)}+\phi_{(t)})$$

where

$A_{(t)}$: Amplitude as function of time (t)
$f_{(t)}$: Frequency as function of time (t)
$\phi_{(t)}$: Phase as function of time (t)

It is fully characterised by three time-domain coefficients $A_{(t)}$, $f_{(t)}$ and $\phi_{(t)}$. If we are able to send these coefficient representations of the RF signal directly to the circuit, then we are shifting the RF problem to a pure coding or VHDL-AMS modelling problem.

Our first thought was to pass these three coefficients via PORT SIGNAL of type REAL. The information (amplitude, frequency and phase) must then be assigned to this PORT. Practically we are dealing with a 3-dimensional real vector, which results in a bus with three circuit connections. That means that we have to add two additional dummy (not physical) wires to the schematic representation. This approach is not acceptable because it conflicts with our connectivity verification objective.

Our second thought was to combine the three coefficients into a single mathematical representation. In this case the RF signal can be coded as follows:

$$RFsig = A_{(t)} * (p*m) + f_{(t)} * \phi + f_{(t)}$$

where

p,m: arbitrary integer coefficients

The decoding functions of the three coefficients are:

$$A_{(t)} = RFsig * div(p * m)$$
$$\phi_{(t)} = (RFsig - A_{(t)}) * div\ p$$
$$f_{(t)} = Rfsig - A_{(t)} - \phi_{(t)}$$

where
div: integer divider

This method is inconvenient because a large number of significant digits are required. Practically we need 11 digits for the frequency, 3 digits for the amplitude and 3 digits for the phase; which makes a total number of 17 digits. We have just reached the simulator limit of 15 due to the C code limitation (15 digits used by real double representation). At this point our problem is to reduce the total number of digits required without sacrificing accuracy. Since frequency and phase are linked by the following relationship:

$$\phi_{(t)} = \int f_{(t)}\, dt$$

we can reduce the significant coefficient number from 3 down to 2. The idea is to code only amplitude and frequency, then restore the phase from the frequency. By doing so, the number of required digits is lowered to 14, which is now acceptable by the tool. This means that we are then only dealing with only 2 coefficients. The temptation to use a built-in PORT of type SPECTRUM, which carries 2 variables, but this is still not a good choice, as it requires two wires of connection.

Finally, the new coding with only amplitude and the frequency is:

$$RFsig = int(f_{(t)}) + A_{(t)}/n$$

with
n: arbitrary integer coefficient chosen as $A_{(t)} / n < 1$
int: integer extraction
dec: decimal extraction

This allows a precision of 1Hz for the frequency and 0.01V for the amplitude. The total number of significant digits is now 14, and the decoding functions are:

$$A_{(t)} = dec(RFsig) * n$$
$$f_{(t)} = int(RFsig)$$
$$\phi_{(t)} = \int f_{(t)}\, dt$$

This coding gives satisfactory results. The designer can read the frequency directly by looking at the displayed waveforms where the integer part of the real value represents the frequency and the decimal part represents the amplitude.

VHDL-AMS modeling: RF signal coding

The RF signal is actually sampled at 13MHz of the PLL frequency. The following architecture uses a coding with a power of ten (see table below).

1. Digital Control Block

The digital control block is used to configure the chip in a desired functional sequence. The three external inputs allow the programmer to access the six internal registers. The block is left at the gate-level because it does not require significant run time compared to other analogue blocks. For the first time, we are able to program the chip as it would be used in a real application, and to verify that it responds correctly to the programming sequence. Simulation allows us to detect bugs that we may not find otherwise. The top three control signals are CLOCK, DATA and ENABLE, and the test sequence changes every milli-second. We can then observe the state of different registers from the graph.

2. AFRICA Top-level Circuit

On a SUN Ultra60 workstation, it takes 23mins CPU time to run 6ms of top-level transient simulation of the chip. Conse-

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ARCHITECTURE functional OF VCO IS

QUANTITY   Vin ACROSS VCTRL TO VSSVCO;      --Input voltage
QUANTITY   Vvco    :REAL    :=0.0       ;    --True output frequency
CONSTANT   f0      :REAL    :=3.6e9     ;    --Middle frequency
CONSTANT   deltaf  :REAL    := 160.0e6  ;    --Frequency slope Hz/V
CONSTANT   R       :REAL    := 1.0e-2   ;    --Amplitude factor for coding
QUANTITY   Ampl0   :REAL    := 0.0      ;    --True amplitude
SIGNAL     Clk     :BIT     := '0'      ;    --Sampling clock
BEGIN
Vvco  == f0 + Vin * deltaf;             -- RF frequency variation
Ampl0 == 2.0 + 0.5 * SIN(3.14e5 * NOW); -- Ampltitude variation
-- VCO output coding --
PROC1: PROCESS(Clk)
VARIABLE Freqcod, Amplcod, output : REAL;
BEGIN
Clk <= NOT clk AFTER (1.0sec/13.0e6);
Freqcod := TRUNC(Vvco);
Amplcod := Ampl0 * R;
output := Freqcod + Amplcod;
OUTPLL <= output ;            -- Output real signal assignment
END PROCESS;
END ARCHITECTURE;
Simulation Results
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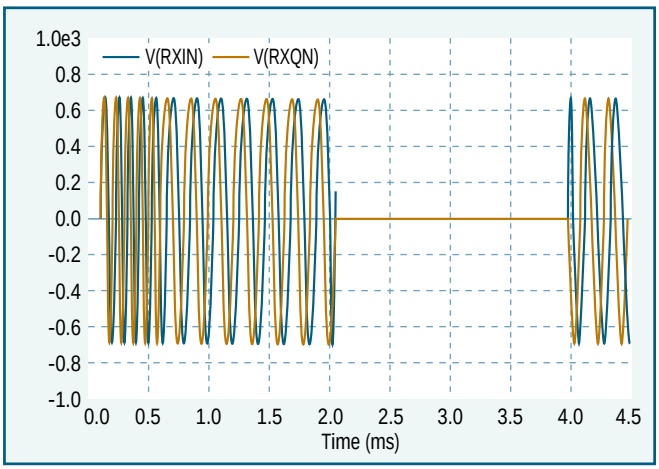

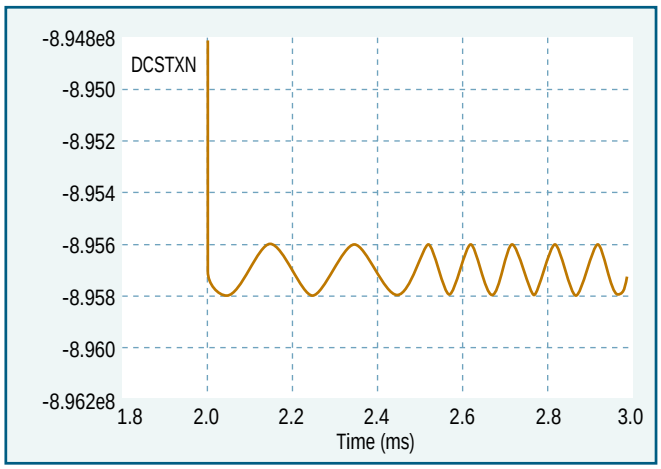

Figure 5 (above left): Receiver output signals and Figure 6 (above right): Transmitter output signals

quently we are very satisfied with the efficiency of the behavioural modelling. With such speed improvements, the simulation can be used to develop test patterns and to extract test signals for the production test group.

In figure 5, the two signals RXIN and RXQN are taken from the receiver outputs. They are 90º shifted baseband signals. The chip is first performing GSM reception up to 0.5ms, then it switches to DCS reception up to 2ms. Notice that there is no reception when the system first starts up and runs for 0.1ms. This represents the PLL locked phase. After 2ms, we switch to DCS transmission mode. The BB signals become silent when the DCSTX output signal taken from the transmitter output starts to swing.

Conclusion

We have successfully simulated the complete transceiver using VHDL-AMS and ADMS. We have also implemented a new methodology to simulate a RF chip at the top-level and our three objectives are fully met. The connectivity has been checked. The functionality checking including power up and power down allows us to detect any errors. So far we have only simulated using an ideal RF signal but the next step is to improve our models with more sophisticated coding to emulate a "real" communication channel. Also we would like to use the simulation to develop a complete test pattern for production test. Despite some difficulties due to the current limitation of VHDL-AMS in the maximum number of significant digits allowed and the constraint of the schematic representation (no dummy wires accepted), we were able to achieve these results with some modelling creativity.

It is clear that VHDL-AMS is reliable and suitable for top-level full chip verification. This should help to create a new kind of job in the future - the VHDL-AMS modelling expert. We also urge test vendors to support this new standard in their virtual test solution.

References

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